Reflectionless Broad-Band Matching Networks Using a Diplexer Approach

Thomas G. McKay

Harris Microwave Semiconductor
1530 McCarthy Blvd
Milpitas, California 95035

1.0 Abstract

A method is presented for generating networks which match an RC load with prescribed gain equalization while simultaneously providing good match. The technique involves the synthesis of two network conductance functions, one of which forms the input conductance of the matching circuit, and a second network which realizes the complimentary conductance. When placed in parallel, the resulting network provides constant, real input impedance, and when driven from a resistive source, provides intended gain equalization. This method has potential advantage over the classical method of balanced, reflection-equalized amplifier networks, for reduced size and lower loss, and is ideally suited for MMIC application since the need for physically large couplers is eliminated. This method preferable over the present heuristic lossy-match approaches, since it is theoretically sound and permits optimal gain-bandwidth design.

2.0 Introduction

The traditional method of broadband MESFET amplifier matching network design employs lossless ladder networks on the input and output of the device. These networks are typically designed using either the analytical techniques first put forth by Mellor[1] or by using Carlin's numerically-oriented real-frequency technique[2]. Presuming one is interested in the maximum available gain of the device, the network will provide conjugate match, or nearly so, at the high end of the band. Since the matching networks are lossless, the reflection coefficient of the amplifier must increase with decreasing frequency; reflection is the mechanism for equalization. With the possible exception of the approach of Riddle and Trew[5], which reports on a special case diplexer circuit, analytical methods for lossy match designs have remained somewhat illusive. The approach followed by many is that of Hornbuckle and Kuhlman.[6] This approach is to place a resistor-transmission line series combination in shunt with the input of the device to be matched. The transmission line is $\lambda/4$ long at the high end of the band resulting in the resistor effectively being removed from the circuit. Given that the maximum available gain level and flatness of the resulting network is acceptable, an approximate equivalent circuit is found for the input (typically numerically) and then matched.

While this approach can be effective, as demonstrated in [6], it does not have the theoretical underpinnings of the reactive match approach. It is not clear, for example, that the addition of the shunt lossy branch does not worsen the gain-bandwidth product available from the device. The approach presented here offers the advantage of maintaining the full gain-bandwidth product of the device, while simultaneously providing match.

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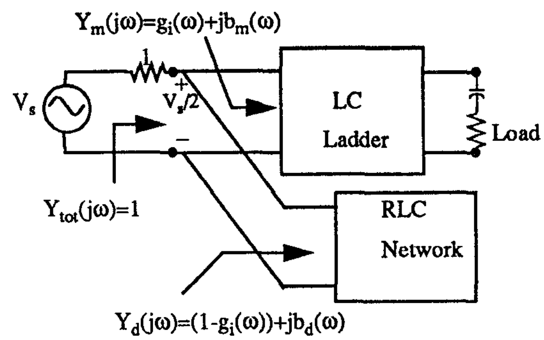
3.0 Diplexer Synthesis Concept

The method reported here is to first carry out a singly-terminated matching network synthesis for the "main arm" network which connects the RC load to a generator. Second, a diplexer arm is synthesized as a two terminal RLC network. Assuming an admittance basis, placing these two networks in parallel results in a constant, matched, input resistance, which, when driven from a resistive source results in the desired characteristics of sloped insertion loss and match.

A singly-terminated synthesis is one which is carried out assuming the source is a voltage or current source as opposed to a power source with an associated resistance. Restricting the discussion to the ostensibly more practical voltage-admittance case, we have the power delivered to the load as $P_{del} = \frac{1}{2}V^2 g_i$, where g_i is the input conductance of the singly-terminated matching network, and V is the peak voltage of the source. The function $g_i(\omega)$ is the function which must conform to Bode's limitation for resistive loads with parasitics. While the expression of the gain-bandwidth limitation is usually expressed in terms of the reflection coeficient, it is not difficult derive forms of the limitation appropriate for the singly-terminated case[5], in which a reflection coeficient is inconvenient to define.

The "diplexer arm" conductance is generated such that when it is added to the main arm conductance, the result is a constant 1 ohm (normalized). The main arm can be realized with an LC ladder; it is a singly terminated sloped-bandpass network. The diplexer arm is not a ladder, since it is a sloped-band reject type response. It is, however, realizable as a general RLC network since the network function is positive real, as will be shown. The resulting network is shown in Figure 1.

FIGURE 1. Diplexer Matching Approach.



4.0 Details of the Method

The input conductance of this network is generated in the manner used by Mellor[1] for reflection-equalized networks. The bandwidth, slope, ripple and order of the desired response on the main arm network determine its conductance function:

$$g_i(\omega) = \frac{\omega^{2s}}{1+\delta^2 T_n^2\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)} \qquad \text{(EQ 1)}$$

where

$$\omega_o = \sqrt{\omega_{upper}\omega_{lower}} \qquad \text{(EQ 2)}$$

is the center frequency,

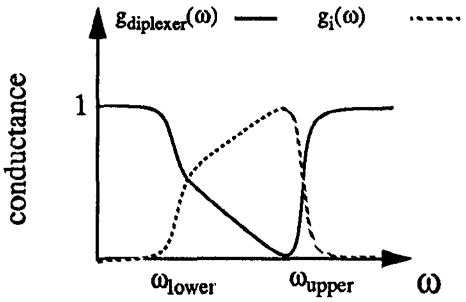
$$\omega_{upper} = 1\frac{rad}{s}, \qquad \text{(EQ 3)}$$

and T_n is the n - th order Tchebychev polynomial. The slope parameter, s, dictates the slope of the gain equalization. The ripple is given by δ and ω is radian frequency. This is essentially an adaptation of Mellor's sloped insertion loss functions adapted for singly terminated design. The diplexer conductance function is given in (EQ 4).

$$g_{diplexer}(\omega) = 1 - g_i(\omega) \quad \text{(EQ 4)}$$

Note that non-integral slope approximations can also be obtained[1]. Note that since $g_i(\omega) \leq 1$, $g_{diplexer}(\omega) \geq 0$. Figure 2. depicts qualitative behavior of the diplexer and main arm conductances.

FIGURE 2. Sketch of the main and diplexer arm conductances.



These conductance functions are the real part of the admittance functions of the two networks. Determining the admittance functions $Y_{main}(s)$ and $Y_{diplexer}(s)$ is done using the Gerwertz method,[4] which is an algebraic procedure for determining Y(s) from $g(\omega)$. The main arm network can be synthesized using zero shifting, resulting in a ladder network. The diplexer arm can be synthesized using, for example, the technique of Bott and Duffin,[3] which will always result in a network not requiring mutual inductance. Note that the diplexer arm is a general RLC network and will in general contain more than one resistor.

The parallel combination of the two networks, when properly synthesized, will always result in cancellation of the imaginary parts of the admittance, as is easily shown. Since the real part of the input admittance of the parallel network is a constant, the input susceptance of the parallel network will automatically be a constant, equal to zero, by the susceptance theorem:

$$b_{total}(\omega) = \frac{\omega}{\pi}\int_0^{\infty} \frac{g_{total}(y)}{y^2 - \omega^2} dy \quad \text{(EQ 5)}$$

$$b_{total}(\omega) = \frac{\omega}{\pi}\int_0^{\infty} \frac{1}{y^2 - \omega^2} dy = 0 \quad \text{(EQ 6)}$$

Realizability of the networks is assured by constraining the conductance functions to be valid network function real-parts. This is assures the complex input admittances will be positive real.

A real function $R(\omega)$ of a real variable ω is the j-axis real part of a positive real function F(s) if and only if[4]:

1. $R(\omega)$ is an even rational function with real coefficients
2. $R(\omega)$ is bounded for all ω.
3. $R(\omega) \geq 0$ for all ω.

Condition 1 is satisfied by the choice of realizable approximation functions (such as T_n). Condition 2 is true for the type of network considered here, as is apparent by considering Figure 2. Condition 3 is satisfied by not allowing g_i to go above 1 S.

5.0 Numerical Example

In order to demonstrate the theory of the previous section, a numerical example is computed, showing the generation of $Y_{main}(s)$ and $Y_{diplexer}(s)$ from the $g_i(\omega)$ and $g_{diplexer}(\omega)$. These admittance functions are seen to be realizable, by examining the location of their poles and zeros. Upon generating these functions, they are evaluated for $s/j=\omega$ for 0.2 to 2.0 rad/sec, and added, demonstrating that the imaginary parts of these two admittances cancel, and their real parts add to unity.

As a practical, tractable example, the case of s=1, n=2, ω_{lower}=0.3 is considered. The admittance functions, generated from the conductance functions using the equations and methods discussed above, are as follows:

(EQ 7)

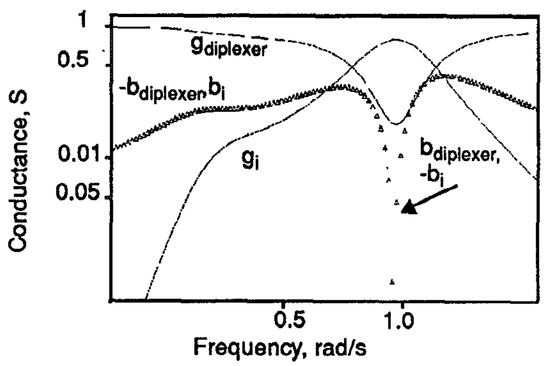
$$Y_{diplexer} = \frac{s^4 + 0.299s^3 + 1.01s^2 + 0.180s + 0.090}{s^4 + 0.230s^3 + 1.14s^2 + 0.767s + 0.090}$$

(EQ 8)

$$Y_{main} = \frac{0.468s^3 + 0.128s^2 + 0.0502s}{s^4 + 0.767s^3 + 1.139s^2 + 0.230s + 0.090}$$

Examination of the poles and zeros of these functions reveals that they are left-half plane and simple. The real part of these functions, computed for $s=j\omega$, $\omega = 0.2$ to 2 rad/sec is shown in Figure 3.

FIGURE 3. Sloped input conductance and diplexer conductance for a lower frequency of 0.3, a slope factor of 1 (6 dB/octave), and a second order Tchebychev characteristic. The suceptances +/- b_i, and +/- $b_{diplexer}$ are plotted to show that their sum is zero.



6.0 Acknowledgments

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7.0 References

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